Techford information

ISO 9001:2015

# VLSI PHYSICAL DESIGN

We work in collaboration with major VLSI Companies for placement


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techford_information

Techford information
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# ABOUT TECHFORD VLSI

Techford VLSI is among the top VLSI training institutes in India. At Techford , we understand the changing demands in the field of VLSI. Our courses are designed to offer students hands-on experience in industry trends. We focus on the overall growth and development of the student. At Techford , our courses are job oriented and our trainers have over 8+ year's industry experience.

Since our inception, we have strived to remain among the best VLSI training institute. We do this through intensive training, affiliation with top-tier semiconductor companies and effective placement programs. Our primary aim at Techford is to connect the student's skill set with industry requirements. We have a very conducive learning environment with modern facilities and tools. Our student's excellent performance in the field has continually ranked us the best VLSI institute in India.

# TECHFORD VLSI UNIQUE FEATURES

## *Expert Trainers and Curriculum*

*We collaborate with trainers who have over 8+ year's industry experience. All our courses are professionally designed and are job-oriented to satisfy the demands of the VLSI industry. Our courses are designed and delivered by Professional in The Industry.*

## *Online/Offline Courses & Affordable Fee*

*Our Online/Offline VLSI courses are designed to ensure that our students gain access to training materials and classrooms at their convenience. We offer state-of-the-art courses at very affordable prices. Our prices are very affordable and competitive with monthly EMI facility.*

## *Powerful EDA Tools*

*We utilize industrial standard EDA tools for hands-on training of our students. During your period as trainee in our VLSI institute, EDA tools are accessible 24×7 through our vpn service.*

## *100% Placement Support*

*At Techford VLSI technologies we provide placement support for our students till they get placed. We collaborate with over 200+ top-level semiconductor companies that provide us with placement opportunities for our students.*

# Physical Design Course Description

Techford VLSI's physical design course is designed to give hands on experience in designing complex chip physical design from RTL to GDSII by utilizing industry standard EDA tools. Course majorly focuses in improving student skill set from the basics and gradually introduce more complex topics with the help of industry standard live projects.

Course material, hand-outs and regular assignments help student to get quick jobs in the semiconductor market. By end of the course you will learn all basics required for interview, physical design flow from floorplanning, power planning, placement, clock tree synthesis and physical verification.

## LEARNING OUTCOME

- Get hands-on experience in physical design from RTL to GDSII by executing industry standard live projects.
- Gain deep knowledge in chip design concepts such as floor planning, power planning and building various type of clock trees.
- Acquire skill set in Static Timing Analysis and Synthesis.
- Learn to verify chip design using all physical verification concepts.
- Placement ready with improved soft skills and digital basics.

## KEY COURSE FEATURES

- 100% placement and tool support till placement is done.
- 24×7 tool access through vpn.
- Affordable fee and EMI facility.
- Industry live projects under the supervision of 15+ experienced trainer.
- Course material, hand-outs, quizzes, assignments to assist in learning.

## ELIGIBILITY

B.E/B.Tech in EEE, ECE & EIE pursuing or completed.
M.E/M.Tech/M.S in VLSI/Embedded/Microelectronics

## TOOLS & VPN

Synopsys IC Compiler and PrimeTime with 24x7 VPN access to tools

## MODE OF STUDY

Offline, Online – Daily and Weekends

## DURATION : 6 Months

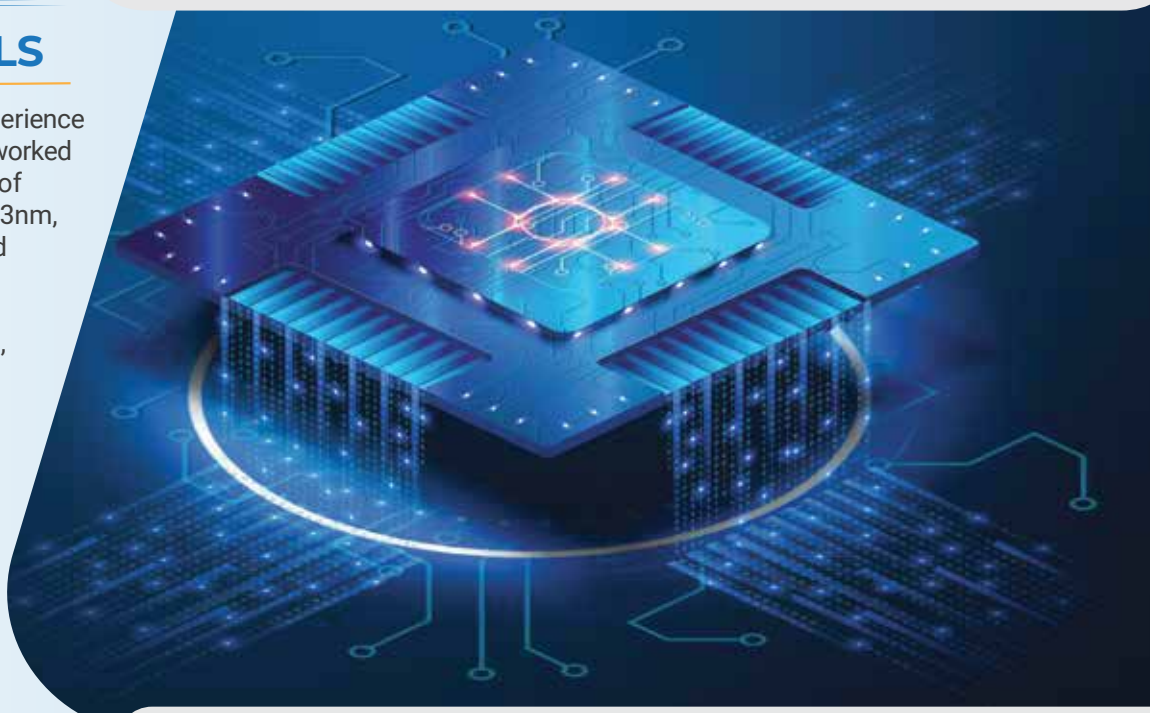
## 200+ LIST OF PLACEMENT COMPANIES

**100% Assured Placement Assistance Till get placed.**

**Typical placement companies:** Capgemini, L&T, HCL, Wipro, Cyient, Samsung, AMD, Synopsys, Tessolve, Micron, Synapse, Cerium, Einfochips, Wafer Space, UST Global, KarMic, Mirafra, Eximius, Sankalp, Insemi, Si2chip, PerfectVIPs, SeviTech, Open Silicon, Atria, Appex, Krisemi, Incise and many more.

## TRAINER DETAILS

Trainer has 8+ years of rich experience in physical design domain. He worked on complete RTL to GDSII flow of cutting edge technology nodes 3nm, 7nm, 10nm from block level and top level. His work involves floorplanning, power planning, clock tree synthesis (CTS), DFM, RC extraction, STA and signal integrity (crosstalk) analysis, Formal and physical verification of complex chip sets such as Modem, Memories, PCIe, PHY. He is also managing an ASIC Backed Design team from RTL to tapeout/Signoff including managing tools flows and design issues. He is our expert for giving hands-on tool and theory knowledge to students.



**COURSE LINK:** https://www.techford.in

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# COURSE CURRICULUM

| S.No | Module Name | Sub-Modules |
|---|---|---|
| Module 1 | Introduction to Electronics, MOSFET & CMOS Theory | Introduction to Electronics and MOSFET Theory |
| | | Introduction to CMOS Process and Circuits |
| Module 2 | Digital Electronics | Binary system and Boolean algebra |
| | | Combinational Circuits |
| | | Sequential circuits - Counters, state machines, shift registers |
| Module 3 | Basics of UNIX/LINUX | Introduction to Unix/Linux Commands |
| | | VI Editor Commands |
| Module 4 | Introduction to ASIC Design | ASIC Flow |
| | | All Stages Discussion |
| Module 5 | Introduction to Verilog | Basic Concepts |
| | | Gate - Level Modeling |
| | | Dataflow Modeling |
| | | Behavioural Modeling |
| | | Tasks and Functions |
| Module 6 | Introduction to DFT | DFT Basics |
| | | Fault Modeling |
| | | Logic and Fault Simulation |
| | | SCAN Design |
| | | Introduction to BIST |
| Module 7 | Synthesis | Inputs and Outputs understanding |
| | | Constraints development and understanding |
| | | Optimization techniques (uniqify, preserve, flatten) |
| | | Wireload model, PLE, Physical, Spatial |
| Module 8 | Static Timing Analysis Part – 1 | Basic understanding of transition/slew, capacitance, leakage power, internal power, On-Chip-Variation (derate, AOCV, LVF) |
| | | Library file difference NLDM, CCS, ECSM, LVF |
| | | Timing concepts understanding such as setup, hold, recovery, removal, pulse width, clock gating check |
| Module 9 | Static Timing Analysis Part – 2 | PLL jitter understanding and uncertainty calculations |
| | | IO budgeting |
| | | Different Timing Modes understanding |
| | | Introduction to ECO |
| Module 10 | Physical Design | Input files, Sanity Checks and IO placement |
| | | Floorplanning and Power planning concepts |
| | | Placement strategies like region, fence, blockages, pading, bump, dont touch, filler gap, DRV optimization, Buffer tree synthesis |
| | | Clock tree synthesis and clock latency calculations |
| | | Routing design and optimization, antenna Effect and Latch up issue |
| | | ECO Timing closure and implementation cycle |
| Module 11 | Physical Design Verification | Design Rule Checks understanding and importance |
| | | Layout Versus Schematic and difference with respect to LEC |
| | | Electrical Rule Checks |
| | | IR Drop analysis - Static and Dynamic |
| Module 12 | Industry standard Project Execution | Industry Standard Physical Design Live Project |
| Module 13 | Mock Interviews & Personality Development | |